Supercomputing and Mass Market Desktops

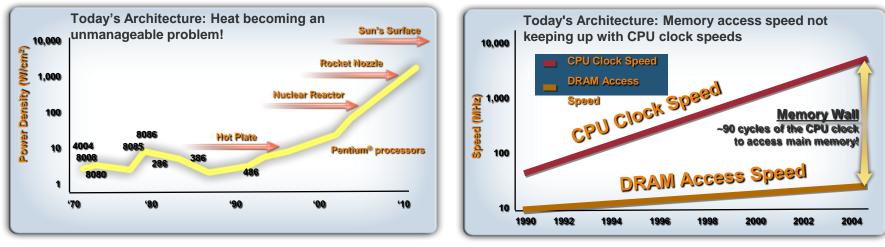
John Manferdelli Microsoft Corporation

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Capabilities on the rise for the end



Hardware Paradigm Shift - 2004



Intel Developer Forum, Spring 2004 - Pat Gelsinger

Modern Microprocessors - Jason Patterson

... we see a very significant shift in what architectures will look like in the future

fundamentally the way we've begun to look at doing that is to move from instruction level concurrency to ... multiple cores per die. But we're going to continue to go beyond there. And that just won't be in our server lines in the future; this will permeate every arch Intel Cancels Top-speed Pentium 4 Chip multicore implementations."

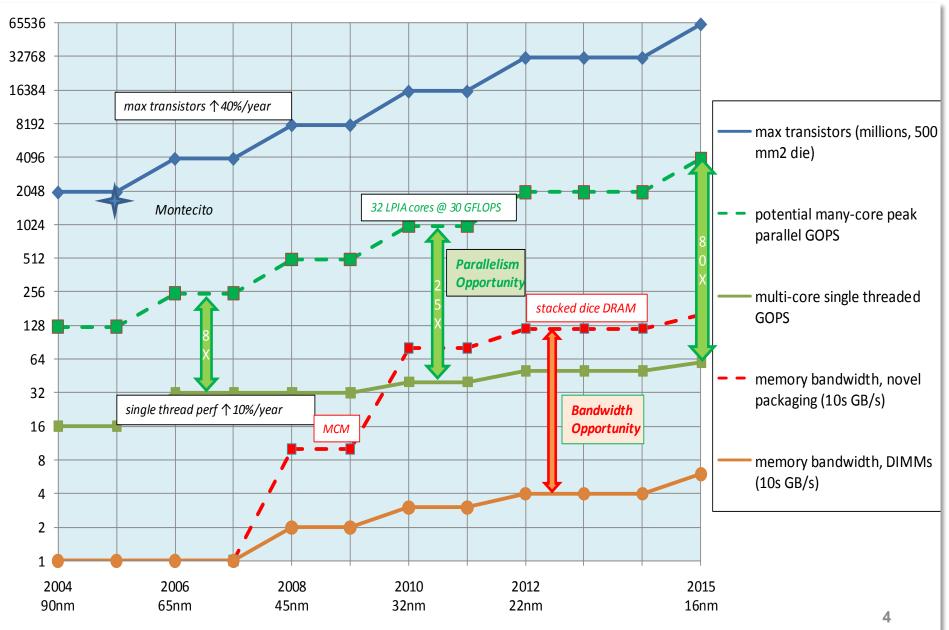
Intel Developer Forum, Spring 2004 Pat Gelsinger **Chief Technology Officer, Senior Vice President Intel Corporation** February 19 2004

Thu Oct 14, 6:50 PM ET Technology - Reuters **By Daniel Sorid**

Intel ... canceled plans to introduce its highest-speed desktop computer chip, ending for now a 25-year run that has seen the speeds of Intel's microprocessors increase by more than 750 times.

----and the second sec

Trends



Lots more computing power

Los Alamos Computing Center? No a single CPU chip.

LPIA	LPIA	DRAM	DRAM		OoO
x86	x86	ctlr	ctlr		x86
LPIA x86	LPIA x86	1 MB cache	1 MB cache		
LPIA	LPIA	1 MB	1 MB	1 MB	
x86	x86	cache	cache	cache	
PCIe ctir	PCle ctlr	NoC	NoC	1 MB cache	1 MB cache
LPIA	LPIA	1 MB	1 MB	1 MB	
x86	x86	cache	cache	cache	
LPIA x86	LPIA x86	1 MB cache	1 MB cache		
LPIA	LPIA	DRAM	DRAM		OoO
x86	x86	ctlr	ctlr		x86

Desktop: 200 mm², 100 W, \$400

DRAM DRAM DRAM DRAM LPIA LPIA LPIA LPIA x86 x86 x86 ctlr ctlr ctlr ctlr **x86** LPIA LPIA 1 MB 1 MB 1 MB 1 MB LPIA **LPIA** x86 x86 cache cache cache cache x86 x86 1 MB LPIA LPIA 1 MB 1 MB 1 MB LPIA LPIA cache cache **x86 x86** cache cache x86 **x86** 1 MB 1 MB 1 MB LPIA LPIA 1 MB LPIA LPIA x86 x86 cache cache cache cache x86 **x86 PCle PCle** NoC NoC NoC NoC NoC NoC ctlr ctlr 1 MB 1 **MB** LPIA 1 MB 1 MB LPIA LPIA LPIA x86 x86 cache cache cache cache **x86 x86** LPIA **LPIA** 1 MB 1 MB 1 MB 1 MB **LPIA LPIA** x86 x86 cache cache cache cache **x86** x86 LPIA 1 MB 1 MB 1 MB 1 MB LPIA LPIA LPIA cache cache x86 x86 cache cache x86 **x86** LPIA **LPIA** LPIA **LPIA Custom acceleration** x86 x86 x86 **x86**

Ultra-Mobile: 40 mm², 5 W, \$50

LPIA	1 MB	1 MB	DRAM
x86	cache	cache	ctlr
LPIA	1 MB	1 MB	PCle
x86	cache	cache	ctlr

Server: 350 mm², 120 W, \$2000

(2008 45 nm process)

Many Core in a Nutshell

- 1. We believe user experiences will benefit from 100 fold improvements in computational power.
- Because of physics, you won't get this power from frequency scaling or programmer transparent hardware like ILP. The only way is parallelism.
- 3. Chips with many *heterogeneous* cores can be manufactured now. Only with chips like this can such performance scaling continue.
- 4. There are difficult but solvable issues related to memory bandwidth and I/O for this to work well over-all.
- 5. There are other benefits from such chips like good power and manufacturing characteristics .
- 6. Application of such hardware does not appear to be limited by any intrinsic lack of parallel algorithms.

Manycore Induced Hard Problems

Constructing parallel applications

- Encapsulating parallelism in reusable components
- Integrating concurrency & coordination into existing programming languages
- Raising the semantic level to eliminate sequencing
- Reducing the complexity of debugging, tuning and testing

Executing fine-grain concurrent applications

- Managing large amounts potential concurrency
- Supporting lightweight transactions
- Interoperating with legacy thread model and interfaces
- Evolving hardware to effectively support parallel programs

Coordination of system resources and services

- Assigning resources securely
- Hosting concurrent operating environments
- Managing resources cooperatively
- Providing concurrent system services
- Managing heterogeneous resources

Manycore Stack

Applications

Libraries

Languages, Compilers and Tools

Concurrency Runtime

OS Kernel

Partitioning Hypervisor

Hardware

Constructing Parallel Applications

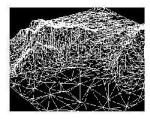
Executing Fine-Grain Parallel Applications

Coordinating System Resources and Services

Developer Impact

Programming Abstractions										
Asynchronous Agents	Concurrent Collections	Transactions								
 Existing Languages Data Parallel Extensions Transactions API for messaging 	 Infrastructure ➤ Transaction & Parallel Safe > Numerical Libraries > Declarative Languages 									
Developer Tools										
Visual Designers Agents, Dataflow	Diagnostics Debugging & Performance Tuning	Testing & Verification								

Simulating The Physical World



DEM Space Shuttle GTOPO 30 NED (US) Earthsat (Europe) Geo Science (Australia)



Landclass Tiling Textures Satellite Imagery



Vectors Roads Rivers Lakes Coastlines Pipelines Power Lines Etc.



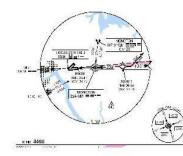
World Weather Seasons Celestial Catalogue Moon Phases Time Zones Magnetic Variation



Autogen Buildings Houses Trees Fences Etc.

Cities

Airports Objects Landmarks Bridges Dams



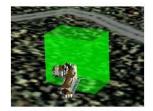
Facilities Data Jeppesen Naviads NOAA Hazards DAFIF FAA



Vehicle Simulation Airplanes Boats Ground Vehicles -Cars & Trucks -Trains Ambient Traffic



Al Paths and Waypoints Jeppesen Navtech



Triggers Text Audio Cameras Animations Cut-Scenes



After Action Review Goals Timing Scoring

Gameplay Simulation



Technical Computing Is Far Reaching

Earth Sciences Life Sciences Social Sciences





Multidisciplinary Research



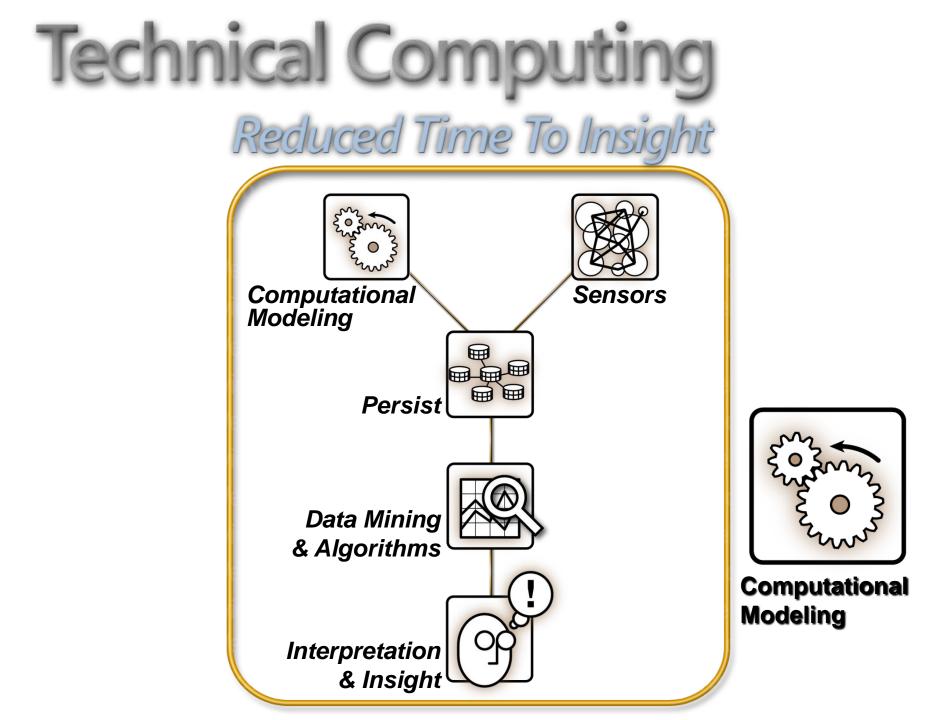
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New Materials, Technologies and Processes





Computer and Information Sciences Math and Physical Science

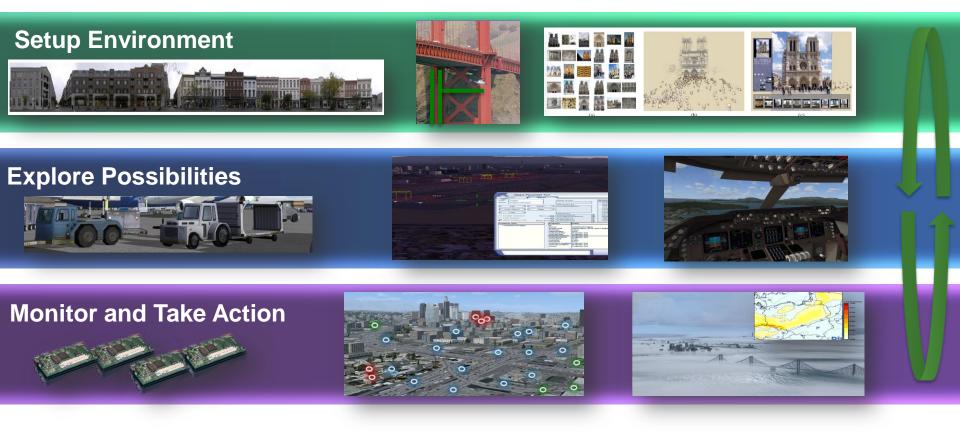


A transformative example

Modeling of the instrumented world

First Responder Scenario (empowering users to make good decisions)

First responders need to quickly and safely experience unfamiliar areas under different disaster scenarios before they deploy into it. For example, earthquakes in San Francisco.



Scenario Features \rightarrow Tech Domains

Modeling the instrumented world

Scenario: First responders need to quickly and safely experience unfamiliar areas under different disaster scenarios before they deploy into it.



Stitching scenes together (2D, 3D)Object recognition in scene✓Interaction (navigation) in sceneLinking scene objects to live data✓Filling in missing information✓Image and video correction✓Long running scene statisticsPersonalization of content✓Simulating physical eventsReal-time scene update

Technology Domains: To realize this scenario, we need to compose these technologies and accelerate their performance at least 10-fold on the manycore client.

The second second second	Machine Learning	Math	Physics	Statistics	Image Processing	3d Modeling	Rendering	Database	Query engine	Index engine	Data compression	Motion Input
		\checkmark			\checkmark	\checkmark	\checkmark	\checkmark				
	\checkmark	\checkmark				\checkmark		\checkmark				
			\checkmark		\checkmark	\checkmark	\checkmark	\checkmark	\checkmark			\checkmark
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		\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	

Tech Domains \rightarrow Platform

Technology Domains

To realize this scenario, we need to compose these technologies and accelerate their performance at least 10-fold of client.

Platform : To compose technology domains and accelerate their performance 10-fold, we need to build the following platform

components

accelerate their performance at least 10-fold on the manycore client	Integrating concurrency into existing languages	Encapsulating parallel- ism in reusable modules	Tools for debugging and profiling parallel code	Support for fine-grain data parallelism	Support for lightweight transactions	Optimization of available bandwidth	System-wide dynamic resource management	Connectivity of services	Managing manycore hardware platform
Machine Learning	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark		\checkmark
Math	\checkmark		\checkmark				\checkmark		\checkmark
Physics	\checkmark	\checkmark	\checkmark	\checkmark		\checkmark	\checkmark		\checkmark
Statistics	\checkmark	\checkmark	\checkmark				\checkmark		\checkmark
Image Processing	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark
3D Modeling	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark		\checkmark
Rendering	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark
Database	✓	✓	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark
Query engine	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	 ✓ 	\checkmark
Data compression	\checkmark		\checkmark				\checkmark		\checkmark
Gesture/Motion Input		\checkmark		\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark

Application/Libraries Architecture

Applications

Application Services

Domain Specific Libraries

> Base Libraries

Personal Assistant Natural UI Program Development Technical Computing **System Design** Information Management Games & Entertainment Biology/Health care Business Intelligence **Robotics**

Speech Engine, Gaming (Physics/AI), Unified Communications, **Database**, Vision, **Machine Learning, Semantic Processing**

Single domain physics, search algorithms, audio/video characterization and extraction, biology simulations, optimization and constraint resolution

Common data structures and algorithms: trees, graphs, tables, sorting, traversal.

System Architecture

